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Evaluating High-Volume, Low-Cost Packaging Choices

Leadless and enhanced leadless leadframe packages provide increased I/O counts and design flexibility, as well as improved thermal and electrical performance.

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Consumer electronics devices continue to see tremendous growth, thanks to a myriad of new technologies, and leadframe packaging is evolving to meet that demand. The need for new and innovative packaging options is paramount.

New advances in leadframe packaging, including quad flat no-lead (QFN), and enhanced leadless leadframe packages, such as the etched leadless package (ELP) using wire bond, flip-chip, stacked die and system-in-a-package (SiP) technologies, continue to be developed.

This article offers insights into ideal deployment for each of these package types, and describes why cost and performance continue to drive package choices, as well as shrinking die and footprint requirements.

Market drivers

Consumer products are always driven by cost. Each new generation is expected to be priced lower, yet offer additional functionality and better performance than its predecessor. But pricing pressures have made costly package material sets, such as ball grid arrays (BGAs), not as desirable because of associated high substrate costs. Another cost consideration is package tooling or any other equipment that must be purchased to bring packages into full production. Tooling up new BGA substrates and creating assembly processes and equipment can introduce substantial cost increases.

With the increase in complexity of ICs for consumer devices, leadframe packages must now offer a higher density of I/Os than those offered in the past with standard leadframe packages. And with ELP's design features, such as multiple rows of I/Os, ground and power rings, the multiple wire-bond loop heights and tighter pitches that were once only offered in BGA packages are now available for leadframe packages. With board space becoming smaller, there is a continued push toward SiP and stacked die that use the more cost-effective leadframe material set.

Thermal and electrical performance remains a key factor in the development of new advanced leadframe packages. The exposed die-attach pad of QFN and ELP provides an enhanced thermal path, moving heat away from the die. With ELP, features such as ground and power rings/bars are now possible for improved electrical performance. Flip-chip technologies that used to be reserved primarily for BGA packages are now used in various leadframe package technologies. These flip-chip die attaches provide improved electrical performance and offer increased reliability, thanks to their robust connections.

Cycle times for consumer products are shrinking, and so are lead times for the development of new package technologies. Ideally, advanced leadframe packages must be production-ready right away and have short lead times for custom tooling. IC manufacturers do not have the luxury of waiting for a package technology to mature. Today, advancements in technologies are measured in cycle times of weeks to months. Consider how quickly your mobile phone, camera or MP3 player become "yesterday's" technology.

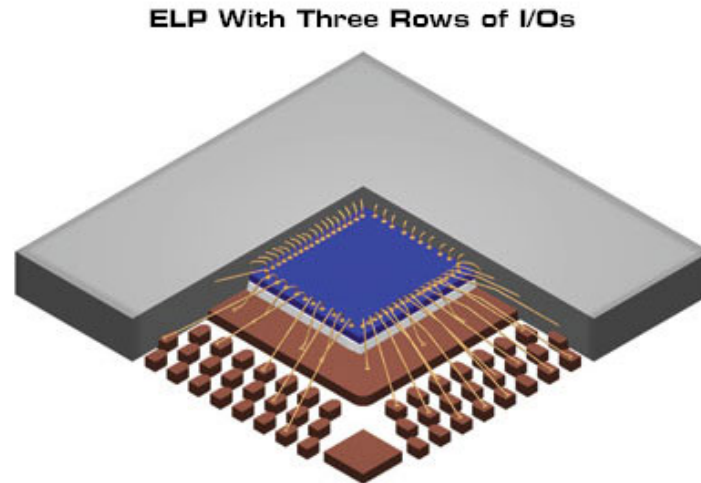
IC manufacturers are hesitant to move their devices to packages that are not proven or in full production. There is no desire to go through a learning curve with the semiconductor and test services (SATS) supplier. Customers prefer a variation of a current package type that meets their evolving device requirements. The ELP is an example of taking a proven technology, the QFN package, and being innovative with the process to create a multirow QFN, while using virtually the same assembly process.

How are SATS companies taking all of these factors into consideration and adapting package portfolios to meet these challenges? Let's explore packaging options, such as multirow QFN packaging or ELPs, and drill down into variations like flip-chip leadframe

packages, stacked die leadframe packages and SiP options, such as QFN-MCM.

Multirow QFN packages

Multirow QFN packaging and ELPs offer benefits of a greater I/O density, design flexibility and improved electrical performance (Fig. 1). The small size of these packages, coupled with their thermal and electrical performance, make them well suited for handheld and portable communication applications where high-performance packages are required.

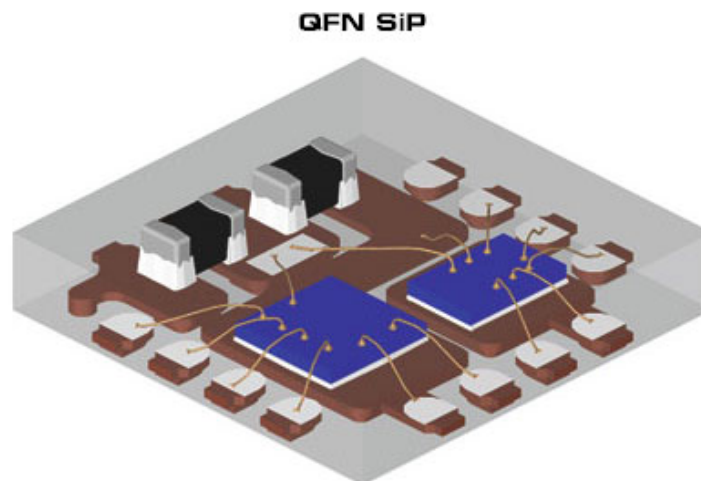


1. The etched leadless package (ELP) takes quad flat no-lead (QFN) packaging to the next level with multiple rows of I/Os and a smaller footprint.

ELP offers flexibility for increased I/O integration and delivers strong interconnectivity from chip to board, allowing for thermal and electrical enhancements with robust reliability. Its multirow capability provides a cost advantage per I/O that is significant when compared with QFN and two-layer laminate package options. Specifically, ELPs can be configured with multiple rows of leadframe posts and power/ground ring options, along with the ability to isolate signal pads and enable I/O signal routing that standard QFNs cannot offer. This provides increased electrical performance with shorter wire lengths, which reduces wire inductance. Overall, the package has a higher I/O count in a smaller package.

SiP leadframe packages

QFN SiP technology has emerged as a low-cost alternative to substrate-based multichip modules (MCMs) and system-on-a-chip (SoC) designs without a drop in reliability (Fig. 2). These SiP solutions offer superior flexibility, which enable wireless manufacturers to more easily support multiple standards, modes and technologies.



2. The QFN system-in-a-package (SiP) provides a higher level of integration, while decreasing the number of components.

What are the ideal deployment scenarios for QFN? The number of IC elements is in direct correlation with the complexity of the circuit functionality. If a product must be integrated in a wide range of applications, the number and intricacy of the challenges are amplified. The packaging industry has learned that it is virtually impossible to put all of this functionality on one IC. This puts package assemblers in a situation where they must take ICs and passives from several suppliers, resulting in the need to design and assemble this circuitry on the motherboard to support the required functionality. By implementing SiP technology, the complexity is transferred to the SiP instead of the system's motherboard.

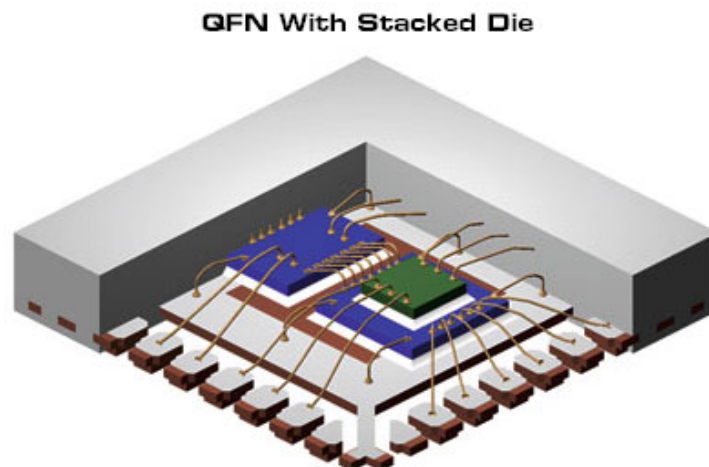
The most important benefit of SiP technology is the integrated functionality of adding the support circuitry to the SiP. Most OEMs are currently downsizing their manufacturing operations in cost-cutting measures, demanding that their component suppliers provide a value-added product. These OEMs are now turning to packaging subcontractors as a value-added resource for addressing innumerable technical challenges associated with SiP technology.

OEMs have discovered that with outsourcing the assembly of SiP, they can specify a single integrated component instead of a discrete active device plus multiple passives.

This integration can be implemented across multiple platforms to give the OEM the benefit of economies of scale that translate into lower costs. By using subcontractors to perform assembly tasks, the normal overhead associated with SiP manufacturing is moved to a lower-cost operating center. And because the subcontractor builds for multiple customers, the OEM is only charged for its portion of the lines. As the OEM's volumes undergo inevitable seasonal or market-driven variations, there is no longer a non-revenue-generating overhead burden.

Stacked die leadframe packages

Shrinking sizes of consumer applications have placed system board space at a premium. With stacked die leadframes, the package footprint stays the same and allows for additional functionality (Fig. 3). This functionality is added by increasing package efficiency in the Z direction. In turn, these single device packages can be combined to free up space on a printed circuit board (PCB).



3. The QFN stacked die SiP is an ideal solution for space-conscious designs, offering two or more die in a single package.

Typical stacking configurations include two die (memory and logic) in one package, with the number of packages increasing the stacking to three or four devices. Emerging and future stacked die packages currently contain more than four devices. However, this involves design- and assembly-related challenges, including signal-to-lead compatibility and die-stacking assembly issues like wafer thinning/preparation, die-attach capability/control, epoxy bleed, outgassing, low-loop requirement with high consistency, wire bonding on overhang die, etc. This is driving assembly equipment and material advancements in the industry, and special die-attach materials, such as die-attach film and epoxy with spacers, are being used to improve bond line control. As a result, new mold compounds are needed that are compatible with the internal configuration; they must also be able to ensure the highest level of reliability. This, in turn,

is prompting companies to upgrade their assembly equipment, including wire bond machines and die attach, to handle today's assembly challenges.

Flip-chip leadframe packages

Eliminating wire bonds and providing a direct signal path from the bump to the leadframe post, which mates to the PCB, increases the performance of flip-chip leadframe packages, such as etched leadless grid arrays (ELGAs). This improves the reliability of both package types, because they can achieve a higher moisture sensitivity level (MSL) rating. Beyond that, flip-chip leadframes offer improved electrical performance, compared with their wire bond counterparts. This allows for lower inductance, resistance and higher capacitance values to be achieved, as well as a shorter time delay for high-speed applications.

There is also a real estate savings advantage, which is needed in most of today's consumer applications. Manufacturers can now put additional I/Os in a given die size, making it possible to shrink the die and ultimately give more die per wafer, which provides an overall cost reduction.

Conclusion

Manufacturers of existing and emerging wireless and smaller consumer applications are reaping the benefits of these new enhanced leadless packages. Specifically, leadless and enhanced leadless packages provide increased I/O counts and design flexibility, as well as improved thermal and electrical performance, which result in superior package reliability.

ELP and QFN take advantage of the existing infrastructure and use standard material sets, making leadless packages an attractive alternative for many applications, such as cell phones and the portable consumer markets (PDAs, camcorders, cameras and MP3 players). The industry will continue to see lower costs and increased performance, driving packaging choices in an industry that continually demands shrinking die sizes and smaller package footprint requirements.

Author Information

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